REMARKS

Claims 1-12, 13 and 15-23 are pending in this application. Claim 16 has been amended. Care has been taken to avoid the introduction of new matter. For the following reasons, this application stands in a condition for allowance.

Claims 1-12 stand allowed. In response to the amendment filed on March 20, 2003, the Examiner allowed claims 13, 15, 18-19 and 20-21, which Applicant acknowledges with appreciation.

The Examiner newly rejects claims 16, 17, 22, and 23 under 35 U.S.C. § 102(e) as being anticipated by Kuwano et al. (U.S. Patent No. 6,571,311 B2). The rejection is respectfully traversed.

Kuwano discloses an EEPROM having a simplified circuit structure accomplished by eliminating complex built-in sequencer circuits. More specifically, as shown by Fig. 3, Kuwano incorporates a register block 102 for receiving data to be written to the EEPROM, address designations for the EEPROM memory, etc. As shown in Fig. 4, the register block 102 may be divided into register block sections; namely, an EEPROM control signal register block 301, an EEPROM address register block 302, an EEPROM data register block 303, and a register address decode block 304. In accordance with an enable signal from the register address decode block 304, control signals, EEPROM address designations, and EEPROM data are read out from respective blocks 301-303 and supplied to the EEPROM memory in a parallel fashion.

Referring to paragraph 4 on page 3 of the Office Action, the Examiner generally refers to Figures 2b, 2c and 3 for teaching the storing steps and memory cell of claim 16, and refers to Figures 6 and 7 and associated text for teaching the first and second registers of claim 16. Basically, the Examiner characterizes the EEPROM as the claimed non-volatile semiconductor memory

device and characterizes the registers of EEPROM data register block 303 as the claimed first and second registers.

To clearly distinguish from the Kuwano reference, claim 16 has been amended to recite "writing said second data stored in said second register to said memory cell to which said first data has been already written."

By contrast, Kuwano discloses a semiconductor device capable of writing a plurality of data to a plurality of memory cells in parallel (*emphasis added*). More specifically, the timing diagram of Figure 5 of Kuwano illustrates the programming operation of the EEPROM memory. Data signals (RA(O:2)) and (RD(O:3)) represent address data and data stored in the register block (Fig. 4), respectively. Data signals (EA(O:7)) and (ED(O:3)) represent address designation and data to be written to the EEPROM memory from the register block. As shown, EEPROM data writing begins at the third activation signal (XEWR). At this time, data is supplied to the EEPROM memory in a parallel fashion. Kuwano neither discloses nor suggests that the second data stored in the second register is written to the memory cell to which said first data has been already written, as amended recites.

Regarding claim 17, Kuwano fails to disclose the step of writing the first data that overlaps with the step of storing the second data in the second register. By contrast, in Kuwano data is to be written to the memory cells or input to the registers only when the RA is "3H" (see Table 1 in column 8 and Fig. 5 in Kuwano). Data input to the registers during other timing are only related to control of the EEPROM in the Kuwano reference. Therefore, in Kuwano, the step of writing the first data does not overlap the step of storing the second data, as claim 17 would otherwise require.

For the foregoing reasons, claims 16, 17, 22, and 23 are deemed distinguishable over the prior art of record, and therefore patentable. Withdrawal of the rejection is respectfully solicited.

If the Examiner has any comments or questions regarding this response or the application in general, the Examiner is encouraged to contact the undersigned in order to expedite prosecution of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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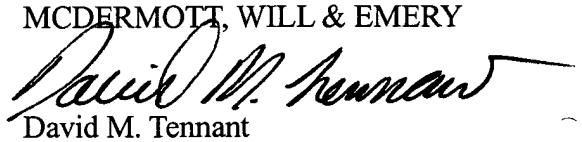

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